Experiment (9)

Binary Counters

9.1 Objectives :

- To learn the difference between synchronous and asynchronous sequential circuits.
- To understand the operation of synchronous binary counters.
- To learn how to design n-bit binary counter using T Flip-Flops.

9.2 Background Information :

Digital circuits can be classified into two types: combinational, in which the circuit outputs are determined by the logical input states at any particular moment; and sequential**,** in which the outputs depend on logical input states and the prior states of outputs. There are two types of sequential circuit, synchronous and asynchronous. Synchronous types use a clock input to drive all the circuit operations. Asynchronous sequential circuits do not use a clock signal, Instead the circuit is driven by the pulses of the inputs.

So far we have considered the combinational circuits in the previous experiments. This experiment will present one important example of sequential circuits which is binary counter. Binary counter is a sequential circuit that moves through a predefined sequence of states. The sequence of states may follow the binary number sequence as shown in the Table 9.1 or an arbitrary manner (non-binary sequence) . The simplest example of a counter is the binary counter, which follows the binary number sequence, this type considered as synchronous sequential circuit. An n-bit binary counter contains n flip-flops and can count binary numbers from 0 to 2^n-1.

A_3	A_2	A_1	A_0
0	0	0	0
0	0	0	1
0	0	1	0
0	0	1	1
0	1	0	0
		.	
		.	
		.	
1	1	1	1

Table 9.1
Binary Count Sequence

To design any synchronous sequential circuit we must follow the following three steps :

1. Deriving the state table and the state diagram.
2. Obtaining the minimum form of the Boolean equations for flip-flop inputs and outputs using K- map.
3. Drawing the logic Diagram.

For instance, consider the design a 3-bit binary counter using T flip-flops, the process will be :

Step 1: State diagram and state table are shown in Figure 9.1 and Table 9.2 respectively :

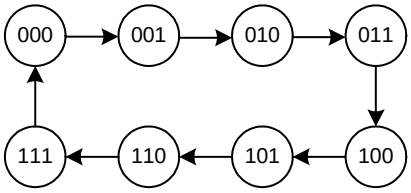

Figure 9.1 State Diagram
for 3-bit Binary Counter

Table 9.2 State table for 3-bit Binary Counter

Present State			Next State			Flip-Flop Inputs		
A_2	A_1	A_0	A_2^+	A_1^+	A_0^+	T_{A2}	T_{A1}	T_{A0}
0	0	0	0	0	1	0	0	1
0	0	1	0	1	0	0	1	1
0	1	0	0	1	1	0	0	1
0	1	1	1	0	0	1	1	1
1	0	0	1	0	1	0	0	1
1	0	1	1	1	0	0	1	1
1	1	0	1	1	1	0	0	1
1	1	1	0	0	0	1	1	1

Because there are 3 flip-flops (T_2,T_1 & T_0), there will be eight states (000,001,… ,111). These states are shown in the state table. The state table shows the present outputs, the next outputs and the flip-flop inputs for each of the eight states. The present state and the next state can be found from the shown state diagram (Figure9.1). The flip-flop outputs can be found using the excitation table of the T flip-flop (see Table9.3). For example , consider the first row in the state table. The unchanged states A_2 and A_1 requiring a T input of 0 and thus T_{A2}=0 and T_{A1}=0. A_0 is complemented in the next state thus T_{A0}=1 .

Q	Q+	T
0	0	0
0	1	1
1	0	1
1	1	0

Table 9.3 Excitation Table for T flip-flop

Step 2 :

Using K-maps , the three simplified Boolean functions for the flip-flop inputs can be found as shown in the Figure 9.2.

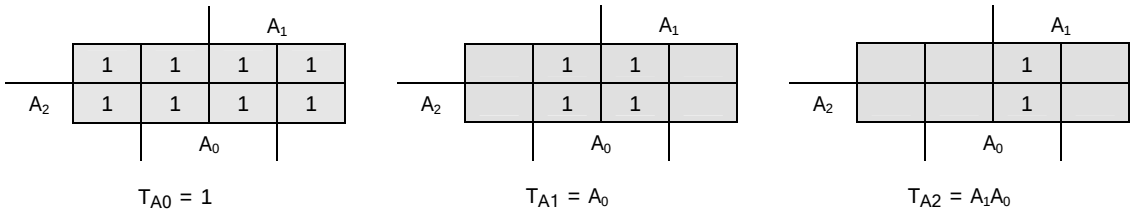

Figure 9.2 K-map for T_{A0} , T_{A1} and T_{A2}

Step 3 :

The logic diagram now can be obtained according to the resultant Boolean equations as shown below.

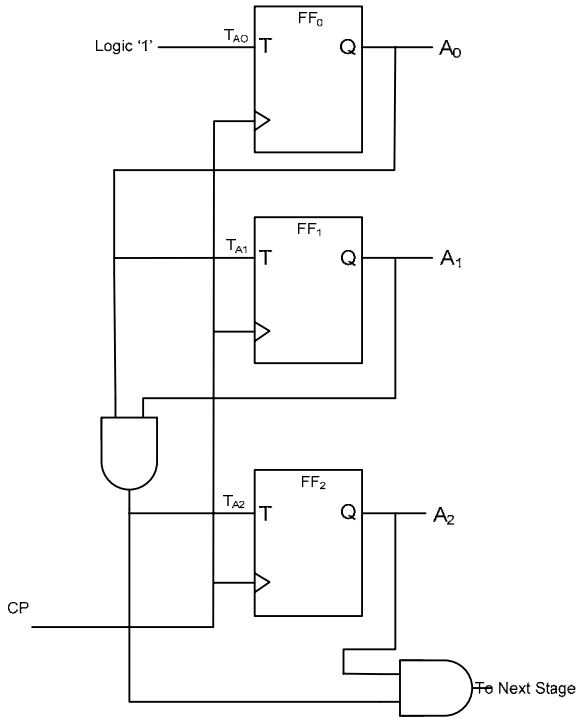

Figure 9.3 Logic Diagram for 3-bit Synchronous Binary Counter

Experimentally , we will construct and test a 4-bit synchronous binary counter. J-K flip-flop can be used instead of T flip-flops because T flip-flop is not commercially available. As we explained in the previous experiment, a T flip-flop can be obtained from J-K type by connecting the J and K inputs together to provide the T input . The logic diagram for 4- bit synchronous binary counter using J-K flip-flops is shown in Figure 9.4.

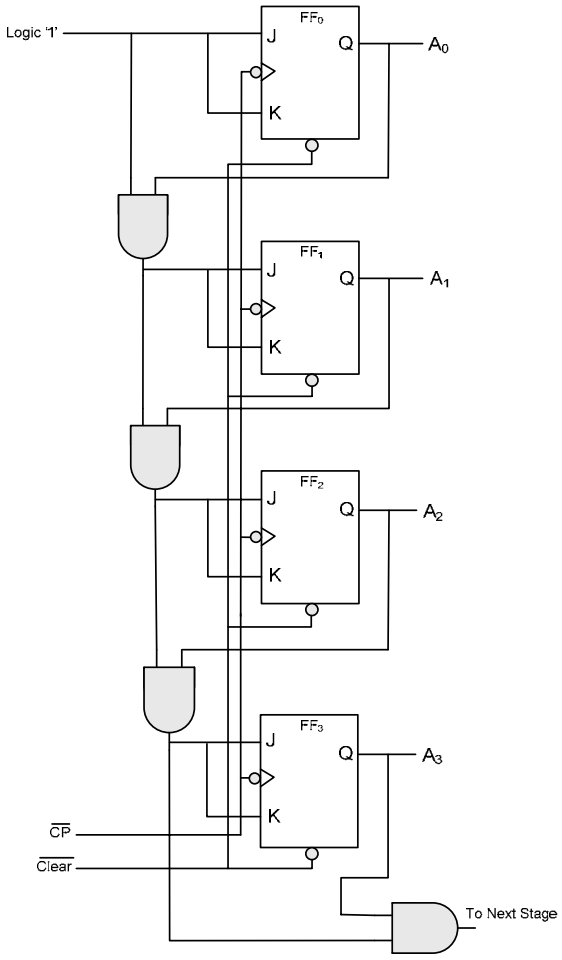

Figure 9.4 Logic Diagram for 4-bit Synchronous Binary Counter

9.3 Equipments Required :

Universal Breadboard
Jumper wire kit
1x 7408 QUAD 2-INPUT NAND GATES
2x 7473 DUAL J-K FLIP-FLOPS WITH CLEAR
1x 7447 BCD-TO-SEVEN SEGMENT DECODERS/DRIVERS
1x Common Anode (CA) Seven-Segment LED Display (MAN72A)
2x Toggle switches or 4-Position DIP Switch.
5x Carbon-film resistors (470Ω)
5x LEDs

9.4 Procedure :

1. Construct the logic circuit of the 4-bit binary counter that shown in Figure 9.4. Use 7447 BCD-to-Seven Segment decoder chip along with a CA 7-segment to display the decimal equivalent of the counter binary outputs. Use 555 oscillator circuit to generate the clock pluses.
2. Once all connections have been done, turn-on the power switch and clear the flip-flops by applying logic '0' to the clear input.
3. Enable the counter and observe its function with each negative-edge in clock pulse input.

Questions :

1. What is the basic difference between a latch and a flip-flop?
2. Implement T Flip-Flop using :
    a) JK Flip-Flip
    b) D Flip-Flop
3. Design a BCD counter to count in the sequence from 0000 up to 1001and repeat . Show all analysis steps.
4. For the binary counter shown in Figure 9.3 , modify the circuit so that the counter goes through the binary states in the reverse order from 1111 down to 0000.
5. Design a 3- bit binary counter that counts in the sequence 0,2,4,6 then back to 0 to repeat the count.
6. Give a summary of the points you have learned from this experiment.

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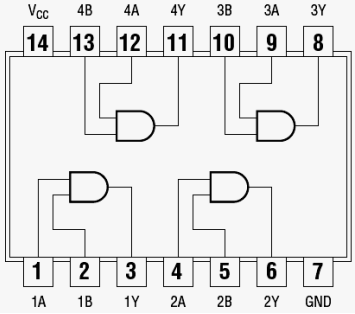
QUADRUPLE 2-INPUT POSITIVE-AND GATES

positive logic:

$Y = A \cdot B$



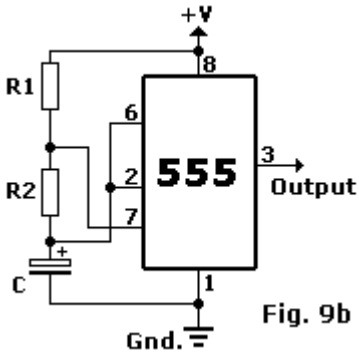


Fig. 9b

$$f = \frac{1.44}{C(R_1 + 2R_2)}$$

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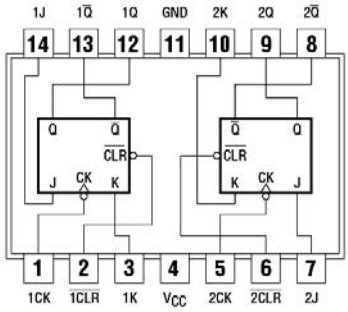
DUAL J-K FLIP-FLOPS WITH CLEAR



FUNCTION TABLE (SN74)

INPUTS				OUTPUTS	
$\overline{\text{CLEAR}}$	CLOCK	J	K	Q	$\overline{Q}$
L	X	X	X	L	H
H	↓	L	L	Q_0	$\overline{Q_0}$
H	↓	H	L	H	L
H	↓	L	H	L	H
H	↓	H	H	TOGGLE	
H	H	X	X	Q_0	$\overline{Q_0}$

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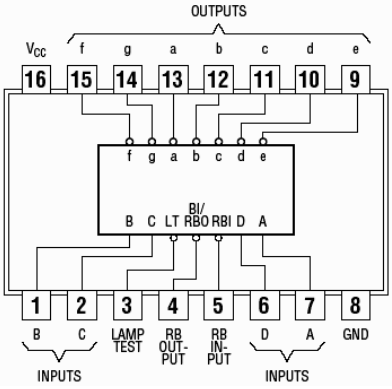
BCD-TO-SEVEN-SEGMENT DECODERS/DRIVERS



FUNCTION TABLE

No.	INPUTS						BI/RBO	OUTPUTS						
	LT	RBI	D	C	B	A		a	b	c	d	e	f	g
0	H	H	L	L	L	L	H	ON	ON	ON	ON	ON	ON	OFF
1	H	X	L	L	L	H	H	OFF	ON	ON	OFF	OFF	OFF	OFF
2	H	X	L	L	H	L	H	ON	ON	OFF	ON	ON	OFF	ON
3	H	X	L	L	H	H	H	ON	ON	ON	ON	OFF	OFF	ON
4	H	X	L	H	L	L	H	OFF	ON	ON	OFF	OFF	ON	ON
5	H	X	L	H	L	H	H	ON	OFF	ON	ON	OFF	ON	ON
6	H	X	L	H	H	L	H	OFF	OFF	ON	ON	ON	ON	ON
7	H	X	L	H	H	H	H	ON	ON	ON	OFF	OFF	OFF	OFF
8	H	X	H	L	L	L	H	ON	ON	ON	ON	ON	ON	ON
9	H	X	H	L	L	H	H	ON	ON	ON	OFF	OFF	ON	ON
10	H	X	H	L	H	L	H	OFF	OFF	OFF	ON	ON	OFF	ON
11	H	X	H	L	H	H	H	OFF	OFF	ON	ON	OFF	OFF	ON
12	H	X	H	H	L	L	H	OFF	ON	OFF	OFF	OFF	ON	ON
13	H	X	H	H	L	H	H	ON	OFF	OFF	ON	OFF	ON	ON
14	H	X	H	H	H	L	H	OFF	OFF	OFF	ON	ON	ON	ON
15	H	X	H	H	H	H	H	OFF	OFF	OFF	OFF	OFF	OFF	OFF
BI	X	X	X	X	X	X	L	OFF	OFF	OFF	OFF	OFF	OFF	OFF
RBI	H	L	L	L	L	L	L	OFF	OFF	OFF	OFF	OFF	OFF	OFF
LT	L	X	X	X	X	X	H	ON	ON	ON	ON	ON	ON	ON