# Exp2: *Designing AND_OR gate*

## Objectives:

The ultimate goal of this experiment is to show how you can write a program using VHDL and how you can synthesis it on Xilinx FPGA.

## Logic Design:

We will use 2-AND gates and 1-OR gate, 4 inputs (a,b,c,d) and 1 output (e).

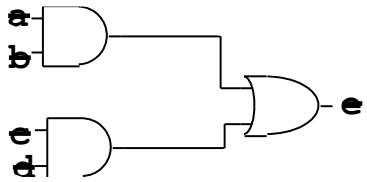
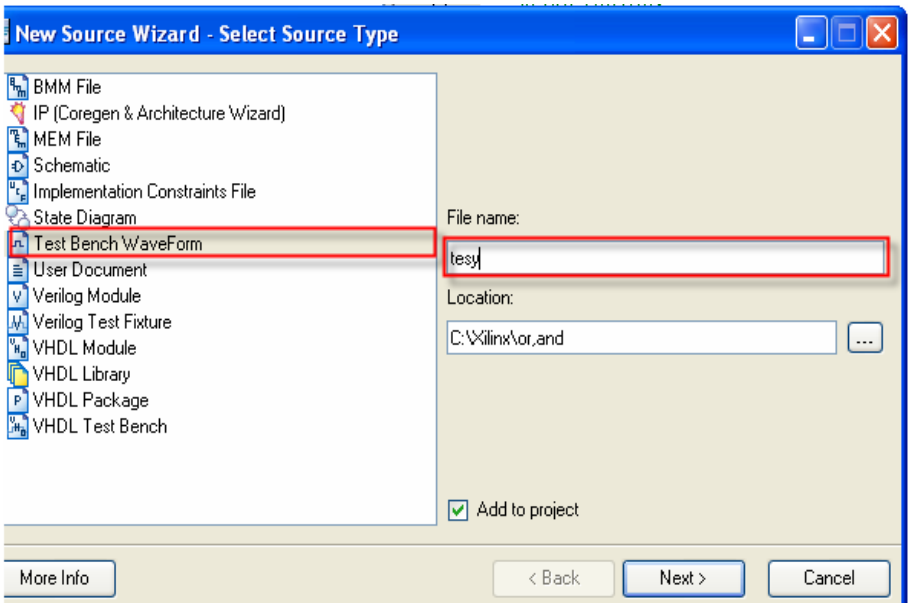



Figure (2-1): AND_OR gates schematic.

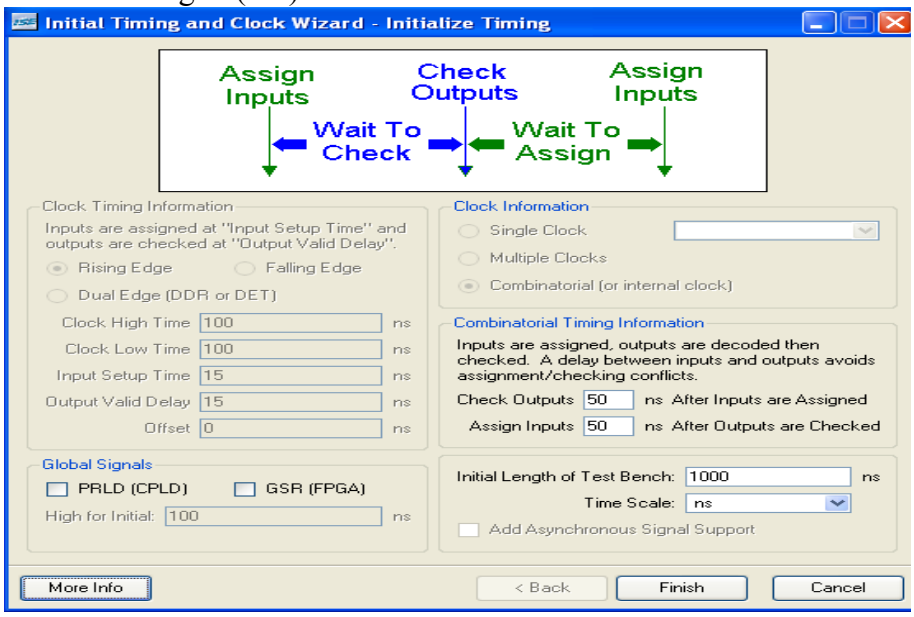
## Simulating with Test Bench Wave Form:

1. To crate a test bench, right-click on the ORAND object then select a new source.
2. Then you will see a new wizard, select Test Bench Wave Form it, then enter the file name and its location, then click next as shown in figure(2-2).



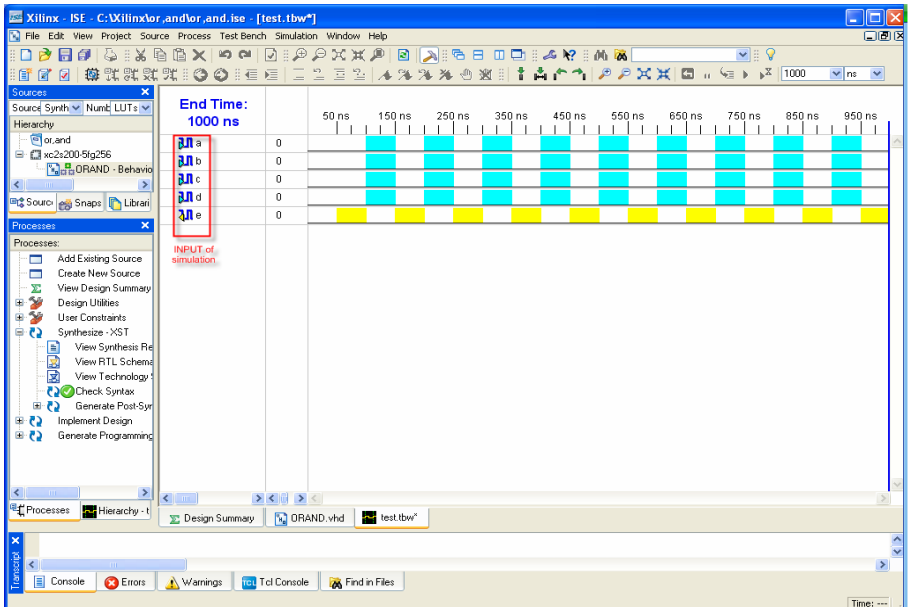

Figure(2-2): Selecting Source Type.

3. After that, you will see the ORAND source code click next and finish.
4. Then, you will see the Initial timing and clock wizard. In this wizard you can limitation the initial length of test bench and time scale and clock information as shown in figure(2-3).




Figure(2-3): Initial Timing Wizard.

5. Then you will see your **test.tbw** windows that you can select form the inputs and the outputs before the simulation.




Figure(2-4): ISE Simulator.

6. Before starting the simulation, right click on ORAND object and select properties. From source properties window, change the association from 'synthesis/Implementation' to 'simulation only'.

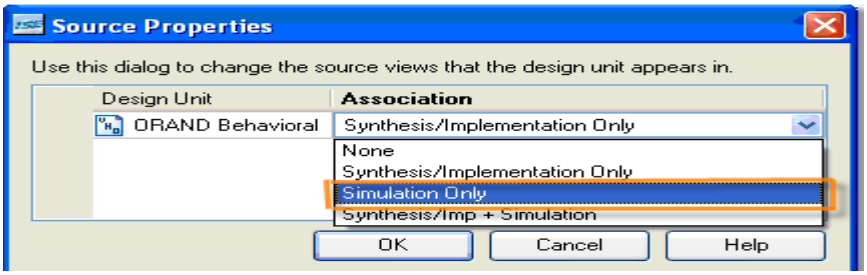
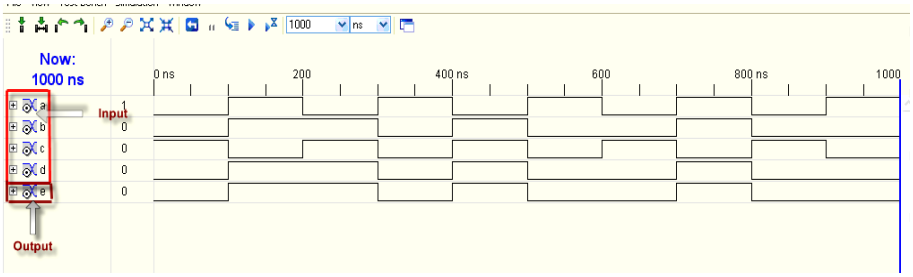



Figure (2-5): Source Properties.

7. Go back to source pane, drop down 'sources for' menu and choose 'Behavioral Simulation'.
8. Double-click on simulate Behavioral model in process pane.
9. Now, you must show the output waveforms.




Figure(2-6): Output Simulation.

## Assigning Pins with Constraints:

| Signals | | Element on XSA-200 Board | XC2S200 FPGA Pin |
|---|---|---|---|
| Input | A | Sw1-1 | P11 |
| | B | Sw1-2 | M10 |
| | C | Sw1-3 | R11 |
| | D | Sw1-4 | N10 |
| Output | E | Segment A | G16 |