# Exp4: *Full Adder*

## Objectives:

The aim of this experiment is designing  a full-adder in VHDL.

## Logic Design:

A Full-Adder is a combinational circuit that forms the arithmetic sum of 3 bits. It consists of 3 inputs and 4 outputs. The inputs (a,b) are variable and (Cin) represents the carry. The output (S) represents the sum of the three bits& (Cout) represents the carry.

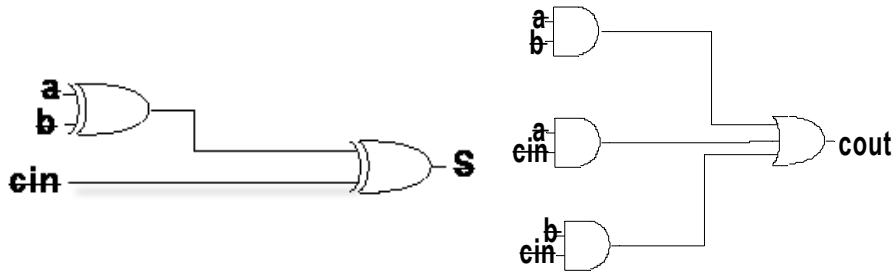


Figure (4-1): Full Adder.

## Assigning Pins with Constraints:

| *Signals* | | *Element on XSA-200 Board* | *XC2S200 FPGA Pin* |
|---|---|---|---|
| Input | A | Sw1-1 | P11 |
| | B | Sw1-2 | M10 |
| | Cin | Sw1-3 | R11 |
| Output | S | Sw1-4 | N10 |
| | Cout | Segment A | G16 |